TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	10/038,162
Filing Date	January 2, 2002
First Named Inventor	Doron Orenstien
Art Unit	2863
Examiner Name	Tung S. Lau
Total Number of Pages in This Submission	18
Attorney Docket Number	42390P10918

ENCLOSURES ***(check all that apply)***

- [X] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Other Enclosure(s) *(please identify below):*

Supplemental Appeal Brief (15 pp)
Return Receipt Postvard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Thomas M. Coester, Reg. No. 39,637 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Thomas Coester
Date	September 13, 2005

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Marilyn Bass		
Signature	Marilyn Bass	Date	September 13, 2005

Based on PTO/SB/21 (04-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wir) 06/04/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($)

Complete if Known	
Application Number	10/038,162
Filing Date	January 2, 2002
First Named Inventor	Doron Orenstien
Examiner Name	Tung S. Lau
Art Unit	2863
Attorney Docket No.	42390P10918

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
☐ Charge fee(s) indicated below, except for the filing fee
☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.
☐ Credit any overpayments

FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) ($)

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Thomas M. Coester	Registration No. (Attorney/Agent)	39,637	Telephone	(310) 207-3800
Signature	Thomas Coester			Date	09/13/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Attorney's Docket No. 42390P10918

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Examiner: **Lau, Tung S.**
Doron Orenstien and **Ronny Ronen**	)	Art Group: **2863**
Application No. 10/038,162	)	
Filed: January 2, 2002	)	
For: **DETERMINISTIC POWER ESTIMATION FOR THERMAL CONTROL**	)	

Assistant Commissioner for Patents
Board of Patent Appeals and Interferences
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL APPEAL BRIEF

Pursuant to 37 C.F.R. § 1.193(b)(2)(ii), Applicants request reinstatement of this appeal following reopening of prosecution by the Examiner. In support of this request to reinstate, Applicants submit the following Supplemental Appeal Brief for consideration by the Board of Patent Appeals and Interferences ("Board"). Please charge any additional amounts due or credit any overpayment to Deposit Account No. 02-2666.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Doron Orenstien and Ronny Ronen, the parties named in the caption, transferred their rights in that which is disclosed in the subject application through an assignment recorded March 6, 2002 (reel/frame number 012449/0210) to Intel Corporation of Santa Clara, California. Accordingly, Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 28-46 are pending in this application. All claims stand rejected. Applicant seeks review of all rejected claims and asks the Board to overturn the rejections based on arguments presented in support of independent claims 28, 35 and 41, and dependent claims 29, 30 and 37.

IV. STATUS OF AMENDMENTS

No amendments to the claims are outstanding or remain to be entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to thermal control for microprocessors. (*See* Field of the Invention.) Embodiments of the invention estimate microprocessor power usage so that a thermal control subsystem can activate throttling mechanisms to avoid high temperatures that can damage the microprocessor. (¶ 8). The power usage estimates are deterministic at a system and application level (¶ 10), so the non-deterministic behavior that plagues thermal-diode-based temperature management schemes can be avoided (¶¶ 4, 5, 10, 33-35).

Power estimates are made by a mathematical function that takes various collected data into account (¶¶ 26, 27). The data may be counts of the number of times certain functional units (such as a floating point processor and cache memory, ¶ 15) are

activated. The function may also factor in other parameters such as the processor's operating voltage and clock frequency (¶ 16). In some embodiments, counter data may be weighted by multiplying counts by weighting factors (¶ 29). Average power consumption may be calculated as a weighted sum over a number of previous estimates of power usage (¶ 31). Embodiments of the invention activate throttling mechanisms when the power consumed exceeds a maximum allowed power (¶¶ 11, 32).

All three independent claims (28, 35 and 41) and dependent claims 29, 30 and 37 are specifically discussed in this appeal.

Independent claim 28 is an apparatus to count the number of times a functional unit of the apparatus is activated and to calculate a deterministic estimate of the apparatus's overall power consumption by a mathematical function that operates on the count (¶¶ 14, 15 and 34).

Dependent claim 29 extends the apparatus of claim 28 to include counting activations of a second functional unit and estimating power consumption by a mathematical function that operates on the two counts and two corresponding weighting factors (¶ 18).

Dependent claim 30 refines the apparatus of claim 28 to include within the deterministic estimate of the overall power consumption, the operating voltage level and current clock frequency of the apparatus (¶¶ 16, 19-20, 30). Dependent claim 37 similarly limits the method of claim 35.

Independent claim 35 is a method of counting the number of times a functional unit of an integrated circuit is activated, and applying a mathematical function to generate a deterministic estimate of the overall power utilization of the integrated circuit based in part on the number of times the functional unit was activated (¶¶ 14, 15 and 34).

Independent claim 41 is a machine-readable medium containing instructions to cause a machine to perform operations comprising counting a number of times a first functional unit of the machine is activated and applying a mathematical function to generate a deterministic estimate of an overall power utilization of the machine, the mathematical function to accept as an input the count of activations of the first functional unit (¶¶ 14, 15, 34 and 36).

VI. GROUNDS OF REJECTION

Claims 28-46 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,719,800 issued to Mittal *et al.* ("*Mittal*").

VII. ARGUMENT

A. Overview of Cited Reference

1. U.S. Patent No. 5,719,800 to Mittal *et al.* ("*Mittal*")

Mittal describes a system to monitor the recent utilization levels of functional units within an IC and calculate an average duty cycle for each unit over its recent operating history (*see* Abstract). Then, if the duty cycle exceeds a sustainable maximum level, functional units can be throttled back to a low-power mode of operation to avoid reliability, heat dissipation or power supply problems (*see* col. 4, lines 19-27).

Several utilization monitoring techniques are suggested, including computing the average duty cycle of a functional unit over the preceding thousand cycles (*see* col. 5, lines 35-38), using an up/down counter as an activity-level register whose contents indicate the current utilization of the functional unit (*see* col. 6, lines 13-16), or adjusting an activity level by a separate increment associated with each possible type of operation (*see* col. 7, lines 12-18).

Mittal proposes reducing power consumption without substantially lowering performance (*see* col. 2, line 65 through col. 3, line 3) by permitting bursts of full-speed computations with a duration less than a threshold to proceed without throttling (*see* col. 5, line 30 through col. 6, line 4). The portion of longer-duration computations that occurs after the threshold is crossed is slowed down so that the activity level remains below a maximum sustainable duty cycle (*see* col. 6, lines 38-49).

No portion of *Mittal*, however, teaches or suggests calculating a deterministic estimate of overall power utilization from inputs including a number of times a functional unit of an apparatus is activated, nor does it make its throttling decisions based on such an estimate.

B. Claims Rejected Under 35 U.S.C. § 102(b)

Claims 28-40 were previously rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,789,037 issued to Gunther *et al.* ("*Gunther*"), while claims 41-46 were rejected under 35 U.S.C. § 102(b) as anticipated by *Mittal* (*supra*). In the Office Action of July 13, 2005, issued in response to Applicants' Appeal Brief, the Examiner abandoned the rejection of the first group of claims over *Gunther* and instead rejected all the claims over *Mittal*.

Although *Mittal*'s system to monitor functional unit utilization and reduce integrated circuit ("IC") power consumption bears some superficial resemblances to Applicants' system for deterministic power estimation for thermal control, it differs in certain key respects. Applicants disagree with the Examiner that *Mittal* discloses all the limitations of the rejected claims, as required for § 102 rejections. The defects of these rejections will be discussed below.

1. Regarding Claims 28 and 35

Claim 28 is drawn to an apparatus comprising a first counter to count a number of times a first functional unit of the apparatus is activated, and a processing unit to apply a mathematical function to yield a deterministic estimate of an overall power consumption, the mathematical function to accept inputs including a value from the first counter. Claim 35 recites a method to generate a deterministic estimate of an overall power utilization of an integrated circuit, comprising counting a number of times a first functional unit is activated and applying a mathematical function to generate the estimate. Both claims contain the idea of calculating a deterministic power estimate based on a count of activations of a functional unit.

Mittal's apparatus includes counters to count activations of functional units, but the counts are not then processed by a mathematical function to produce a deterministic estimate of overall power consumption (nor are the counts themselves such an estimate). Instead, the described counters are operated in an up/down or other complex manner, so that their values reflect recent utilization or duty cycle of the functional unit, not just the number of activations (*see, e.g.*, col. 6, lines 13-26). The recent utilization or duty cycle (also called "activity level") of a functional unit is used to determine whether to activate throttling measures.

The Examiner asserts in the recent Office Action that *Mittal* discloses the claimed mathematical function at col. 6, line 13 through col. 7, line 19, and in Figures 3 and 5. However, Applicants' review of the cited sections (as well as the reference generally) fails to disclose such a function. The design alternatives *Mittal* discusses are ways of operating the up/down counter so that its value directly reflects the activity level of the functional unit. For example, if the counter is incremented by one during each active cycle and decremented by one during each inactive cycle, then limiting the value of the counter to a particular threshold results in the unit being operated at a 50% duty cycle (*see* col. 6, lines 27-32). Figure 3 shows an embodiment of *Mittal*'s invention controlling the power consumption of a cache memory based on the contents of an activity-level register, while Figure 5 shows a power coordinator operating across multiple functional units. Neither figure nor its accompanying description mentions estimating power consumption or utilization. Figure 5 does include a signal captioned "Power Consumption Information" (507), but the description makes clear that this information is the "current activity levels of any or all functional units being monitored," (*see* col. 11, lines 21-22), and not an estimate of power consumption generated by applying a mathematical function to a counter value.

Since *Mittal* fails to teach or suggest at least this element of independent claims 28 and 35, the Board should overturn the rejection of these claims.

2. Regarding Claim 29

Claim 29 refines the computation of the deterministic estimate of overall power consumption to include a second counter of functional unit activations and a weighting factor associated with each counter, where the mathematical function accepts as additional inputs the weighting factors and a value from the second counter to yield a deterministic estimate of overall power consumption. *Mittal* does disclose counting activations of multiple functional units (though not in the sections relied upon by the Examiner) but all of these counters produce information about the current activity level or duty cycle of the functional unit, not an estimate of overall power consumption. Because *Mittal* fails to teach or suggest producing the claimed estimate from the counter values, the Board should overturn the rejection of claim 29.

3. Regarding Claim 30 and 37

Claim 30 refines the apparatus of claim 28, requiring that the mathematical function to yield a deterministic estimate of overall power consumption also accept as additional inputs an operating voltage level of the apparatus and a current clock frequency of the apparatus. Claim 37 provides, in relevant part, similar limitations to the method of claim 35. It is true, as the Examiner observes, that *Mittal*'s Figure 2 includes a "System Clock" signal (element 201), but the description of the figure at col. 8, line 25 through col. 9, line 3, makes clear that the system clock drives the up/down counter 205, incrementing when the floating point unit ("FPU") 206 is active, and decrementing when it is inactive. The most significant bit of the counter is used to control the multiplexer 203, providing the FPU with a full-speed or half-speed clock, depending solely on the recent utilization of the FPU. No estimate of overall power consumption is taught or suggested; the operating speed of the FPU is controlled simply by its recent utilization. In addition, the operating voltage level does not affect the throttling mechanism at all. Therefore, Applicants respectfully submit that the Board should overturn these rejections.

4. Regarding Claim 41

Claim 41 was rejected under 35 U.S.C. § 102(b) as anticipated by *Mittal* in the Final Office Action of February 4, 2005, but Applicants' arguments in the Appeal Brief of June 27, 2005 were not addressed in the most recent Office Action. Although the Examiner has selected different portions of the reference to support the current rejection (col. 6, lines 12 through col. 7, line 19 instead of col. 1, lines 28-67 and Figures 2, 4 and 5) Applicants maintain that a *prima facie* case of anticipation has not been established.

Claim 41 is drawn to a machine-readable medium containing instructions to cause a machine to perform certain operations, including counting a number of times a first functional unit of the machine is activated and applying a mathematical function to generate a deterministic estimate of an overall power utilization of the machine, the mathematical function accepting as an input the number of times the first functional unit was activated. *Mittal*'s system counts the number of times various functional units of an integrated circuit are activated (*see, e.g.*, col. 6, lines 8-26), but the counts are not used to generate a deterministic estimate of overall power utilization. Instead, *Mittal* teaches using the counts to compute a different value, the average duty cycle (*see* col. 5,

lines 30-37). In fact, a significant portion of *Mittal* explores ways of operating the counter so that its value directly represents the current utilization, without requiring further processing.

An unstated premise that seems to underlie the Examiner's position is that there is a necessary relationship between the average duty cycle of a functional unit and the overall power utilization of a chip. The Examiner does not identify any portion of *Mittal* that suggests such a relationship or provide analysis to support the idea that the relationship is inherent in the derivation of the average duty cycle. Furthermore, Mittal *et al.* explicitly state a *different* relationship between the duty cycle and power: at col. 6, lines 47-49, they observe that "the current value of the activity-level register can be thought of as [the functional unit's] *current power deficit*." A power deficit is a different quantity than the power utilization of the machine, so the reference teaches a contrary lesson to the unstated, but necessary, premise. Consequently, the Board should overturn the rejection of claim 41.

CONCLUSION

Based on the foregoing, the Board should **overturn** the rejection of claims 28-46 and hold that all of the claims currently pending in the application under review are allowable.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Dated: September 13. 2005

Thomas M. Coester, Reg. No. 39,637

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025

(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope with sufficient postage, addressed to:

Commissioner for Patents
Mail Stop Appeal Brief – Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Marilyn Bass — September 13, 2005

VIII. CLAIMS APPENDIX

The claims involved in this appeal are presented below.

28. (Previously Presented) An apparatus comprising:

a first counter to count a number of times a first functional unit of the apparatus is activated;

a processing unit to apply a mathematical function to yield a deterministic estimate of an overall power consumption, the mathematical function to accept inputs including a value from the first counter.

29. (Previously Presented) The apparatus of claim 28, wherein

a first weighting factor is associated with the first counter;

a second counter having a second weighting factor is provided, the second counter to count a number of times a second functional unit of the apparatus is activated; and

the mathematical function accepts as additional inputs the first weighting factor, the second weighting factor and a value from the second counter.

30. (Previously Presented) The apparatus of claim 28, the mathematical function to accept as additional inputs an operating voltage level of the apparatus and a current clock frequency of the apparatus.

31. (Previously Presented) The apparatus of claim 28, further comprising:

at least one throttle to alter the overall power consumption of the apparatus, wherein

the at least one throttle is activated if the deterministic estimate of an overall power consumption exceeds a first threshold power level, and

the at least one throttle is deactivated if the deterministic estimate of an overall power consumption falls below a second threshold power level.

32. (Previously Presented) The apparatus of claim 31 wherein the first threshold power level and the second threshold power level are the same.

33. (Previously Presented) The apparatus of claim 28 wherein the first functional unit is one of a floating point unit, a cache unit, and an instruction decoding unit.

34. (Previously Presented) The apparatus of claim 28 wherein the mathematical function accepts as an additional input at least one previous deterministic power consumption estimate.

35. (Previously Presented) A method comprising:

counting a number of times a first functional unit of an integrated circuit is activated and

applying a mathematical function to generate a deterministic estimate of an overall power utilization of the integrated circuit, the mathematical function accepting as an input the number of times the first functional unit was activated.

36. (Previously Presented) The method of claim 35, further comprising:

adjusting the number of times the first function unit was activated by a first scaling factor;

counting a number of times a second functional unit of an integrated circuit is activated;

adjusting the number of times the second functional unit was activated by a second scaling factor; and

supplying the adjusted number of times the second functional unit was activated as an additional input to the mathematical function.

37. (Previously Presented) The method of claim 35, further comprising:

supplying an operating voltage level and a current clock frequency of the integrated circuit as additional inputs to the mathematical function.

38. (Previously Presented) The method of claim 35, further comprising:

reducing the operating voltage level of the integrated circuit if the estimate of the overall power utilization exceeds a first threshold, and

increasing the operating voltage level of the integrated circuit if the estimate of the overall power utilization falls below a second threshold.

39. (Previously Presented) The method of claim 35, further comprising:

reducing the clock frequency of the integrated circuit if the estimate of the overall power utilization exceeds a first threshold, and

increasing the clock frequency of the integrated circuit if the estimate of the overall power utilization falls below a second threshold.

40. (Previously Presented) The method of claim 35 wherein the first functional unit is one of a floating point unit, a cache unit, and an instruction decoding unit.

41. (Previously Presented) A machine-readable medium containing instructions that, when executed by a machine, cause the machine to perform operations comprising:

counting a number of times a first functional unit of the machine is activated, and

applying a mathematical function to generate a deterministic estimate of an overall power utilization of the machine, the mathematical function accepting as an input the number of times the first functional unit was activated.

42. (Previously Presented) The machine-readable medium of claim 41 containing instructions that, when executed by the machine, cause the machine to perform additional operations comprising:

adjusting the number of times the first function unit was activated by a first scaling factor;

counting a number of times a second functional unit of the machine is activated;

adjusting the number of times the second functional unit of the machine was activated by a second weighting factor; and

incorporating the adjusted number of times the second functional unit was activated into the estimate of the overall power utilization.

43. (Previously Presented) The machine-readable medium of claim 41 containing instructions that, when executed by the machine, cause the machine to perform additional operations comprising incorporating an operating voltage level of the machine and a current clock frequency of the machine into the estimate of the overall power utilization.

44. (Previously Presented) The machine-readable medium of claim 41 containing instructions that, when executed by the machine, cause the machine to perform

additional operations comprising averaging the estimated power utilization with at least one previously-generated estimated power utilization.

45. (Previously Presented) The machine-readable medium of claim 41 containing instructions that, when executed by the machine, cause the machine to perform additional operations comprising:

reducing an operating voltage level of the machine if the estimated overall power utilization is above a first threshold; and

increasing the operating voltage level of the machine if the estimated overall power utilization is below a second threshold.

46. (Previously Presented) The machine-readable medium of claim 41 containing instructions that, when executed by the machine, cause the machine to perform additional operations comprising:

reducing a clock frequency of the machine if the estimated overall power utilization is above a first threshold; and

increasing the clock frequency of the machine if the estimated overall power utilization is below a second threshold.

IX. EVIDENCE APPENDIX

No evidence is submitted with this appeal.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings exist.